IRF640, RF1S640,RF1S640SM
18A, 200V, 0.180 Ohm, N-Channel Power Mosfets

These are N-Channel enhansement mode silicon gate power field effect transistors. They are advance power MOSFETs designed, tested, and guaranteed to withstancd a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.
Formerly developmental type TA17422.

Features

- 18A, 200V
- $r_{DS(ON)}$=0.180 Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speed
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature

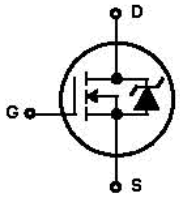
-TB334 “Guidelines for Soldering Surface Mount Components PC Boards”

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRF640	TO-220AB	IRF640
RF1S640	TO-262AA	RF1S640
RF1S640SM	TO-263AB	RF1S640

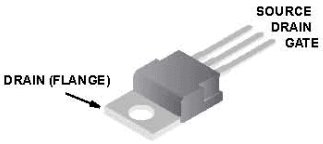
NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in the tape and reel, i.e., RF1S640SM9A.

Symbol

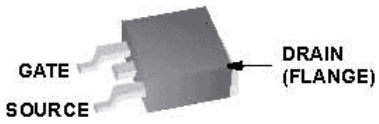


Packaging

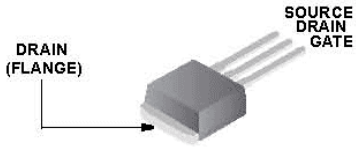
TO-220AB



TO-263AB



TO-262AA



Absolute Maximum Ratings Tc=25℃, Unless Otherwise Specified

	IRF640, RF1S640,RF1S640SM	UNITS
Drain to Source Breakdown Voltage (Note 1)……V_{DS}	200	V
Drain to Gate Voltage (R_{GS}=20k Ω) (Note 1)……V_{DGR}	200	V
Continuous Drain Current……I_D	18	A
Tc=100℃……I_D	11	A
Pulsed Drain Current (Note 3)……I_{DM}	72	A
Gate to Source Voltage……V_{GS}	±20	V
Maximum Power Dissipation……P_D	125	W
Dissipation Derating Factor……	1.0	W/℃
Single Pulse Avalanche Energy Rating (Note 4)……E_{AS}	580	mJ
Operating and Storage Temperature……T_J, T_{STG}	-55 to 150	℃
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Cases for 10s……..TL	300	℃
Package Body for 10s, See TB334……Tpkg	260	℃

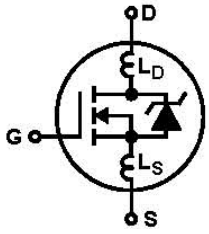
CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. TJ=25°C to 125°C.

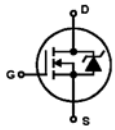
Electrical Specifications Tc=25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown	BV_{DSS}	I_D=250μA, V_{GS}=0V, (Figure 10)	200	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS}=V_{DS}, I_D=250μA	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=Rated BV_{DSS}, V_{GS}=0V	-	-	25	μA
		V_{DS}=0.8 x Rated BV_{DSS}, V_{GS}=0V, T_J=125°C	-	-	250	μA
On-State Drain Current (Note 1)	$I_{D(ON)}$	V_{DS}>$I_{D(ON)}$ x $r_{DS(ON)MAX}$, V_{GS}=10V (Figure 7)	18	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V	-	-	±100	nA
Drain to Source On Resistance(Note1)	$I_{D(ON)}$	I_D=10A, V_{GA}=10V (Figure8,9)	-	0.14	0.18	Ω
Forward Transconductance (Note1)	gfs	V_{DS}≥10V, I_D=11A (Figure 12)	6.7	10	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD}=100V, I_D=18A, R_{GS}=9.1 Ω, R_L=5.4 Ω, MOSFET Switching Times are Essentially Independent of Operating Temperature	-	13	21	ns
Rise Time	tr		-	50	77	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	46	68	ns
Fall Time	tf		-	35	54	ns
Total Gate Charge (Gate to Source +Gate to Drain)	$Q_{g(TOT)}$	V_{GS}=10V, I_D=18A, V_{DS}=0.8 x Rated BV_{DSS} (Figure 14) Gate Charge is Essentially Independent of Operating Temperature $I_{G(REF)}$=1.5mA	-	43	64	nC
Gate to Source Charge	Qgs		-	8	-	nC
Gate to Drain "Miller" Charge	Qgd		-	22	-	nC
Input Capacitance	C_{ISS}	V_{DS}=25V, V_{GS}=0V, F=1MHz (Figure 11)	-	1275	-	pF
Output Capacitance	C_{OSS}		-	400	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Internal Drain Inductance	L_D	Measured From the contact Screw on Tab to Center of Die; Modified MOSFET Symbol Showing the Internal Devices Inductances	-	3.5	-	nH
		Measured From the Drain Lead, 6mm (0.25in) From Package to Center of Die	-	4.5	-	nH
Internal Source Inductance	LS	Measured From the Source Lead, 6mm (0.25in) from Header to Source Bonding Pad	-	7.5	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	1	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation, IRF640	-	-	62	°C/W
	$R_{\theta JA}$	RF1S640SM Mounted on FR-4 Board with Minimum Mounting Pad	-	-	62	°C/W



Source to Drain Diode Specifictions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the integral Reverse P-N Junction Diode	-	-	18	A
Pulse Source to Drain Current (Note 2)	I_{SDM}		-	-	72	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	T_J=25°C, I_{SD}=18A, V_{GS}=0V, (Figure 13)	-	-	2.0	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_{SD}=18A, dI_{SD}/dt=100A/μs	120	240	530	ns
Reverse Recovery Charge	Q_{rr}	T_J=25°C, I_{SD}=18A, dI_{SD}/dt=100A/μs	1.3	2.8	5.6	μC



NOTES:

2. Pulse Test: Pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. V_{DD}=50V, starting T_J=25°C, L=3.37mH, R_G=25 Ω, peak I_{AS}=18A.

Typical Performance Curves Unless Otherwise Specified

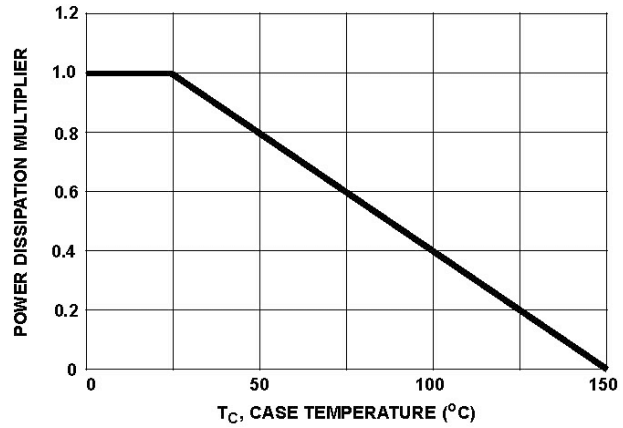


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

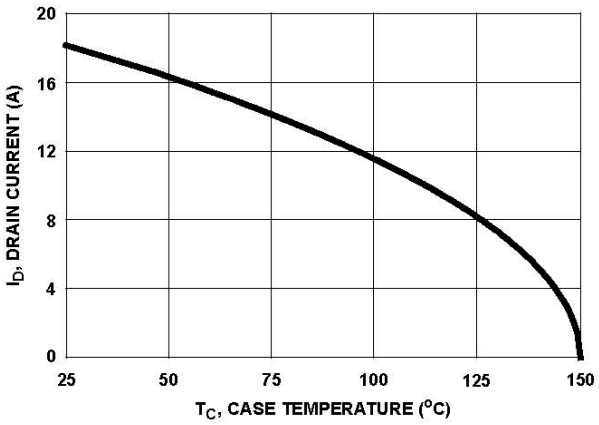


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

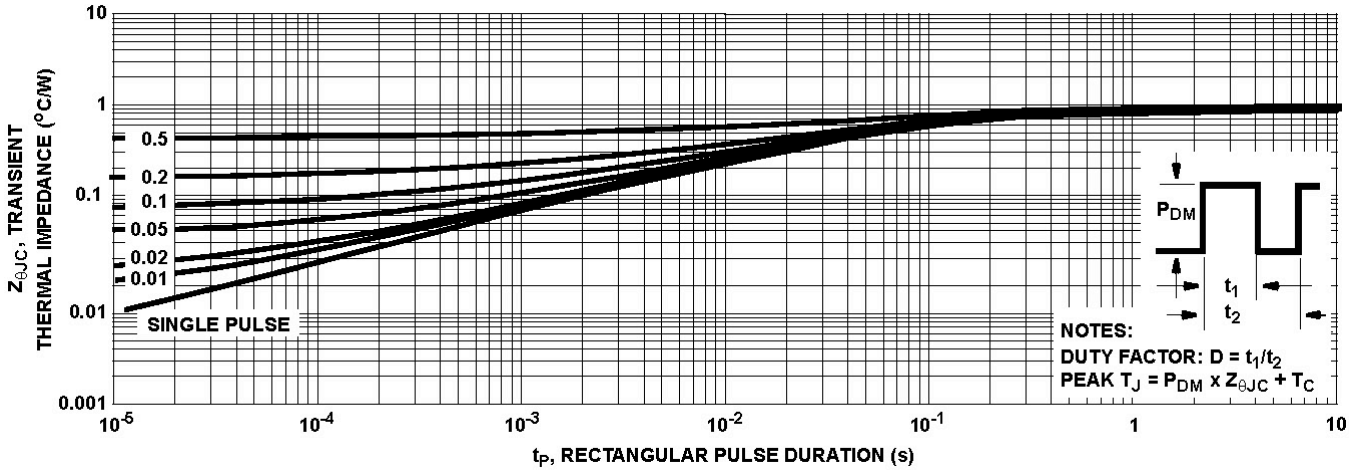


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified (Continued)

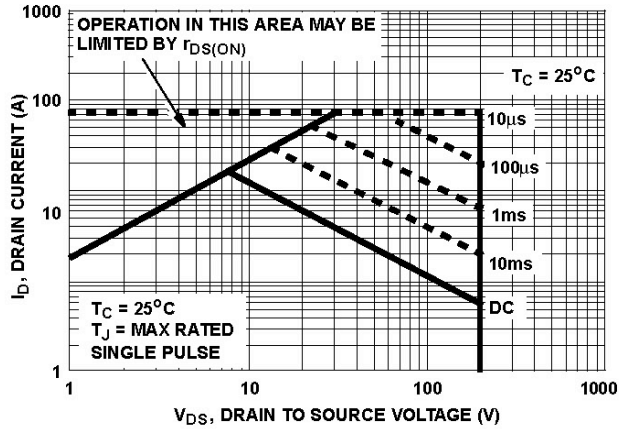


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

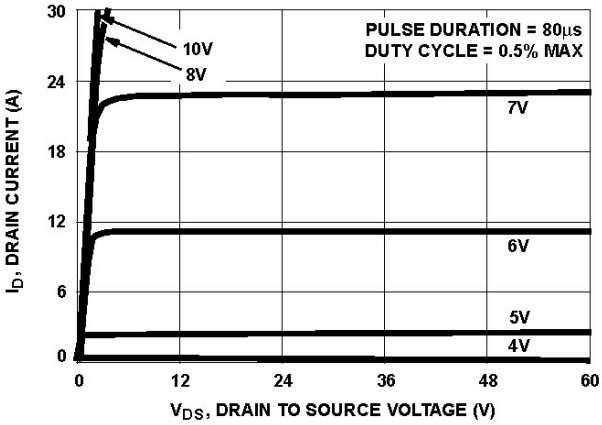


FIGURE 5. OUTPUT CHARACTERISTICS

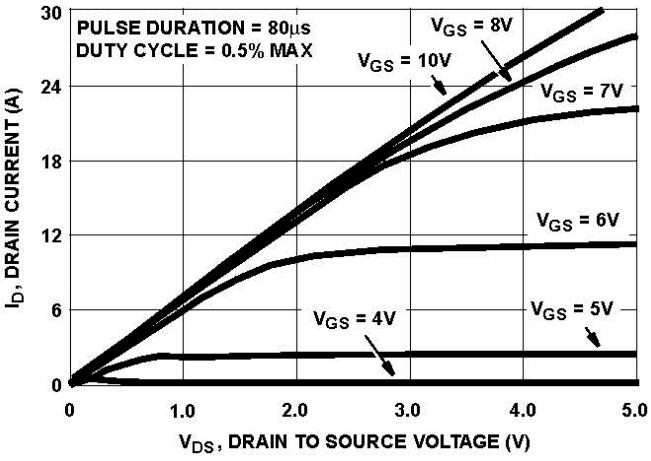


FIGURE 6. SATURATION CHARACTERISTICS

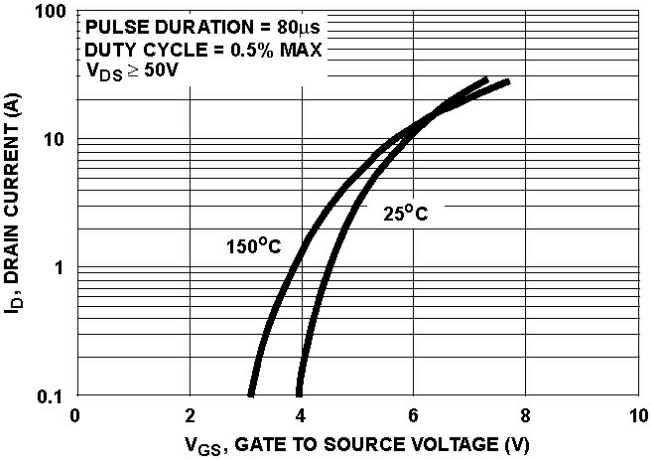


FIGURE 7. TRANSFER CHARACTERISTICS

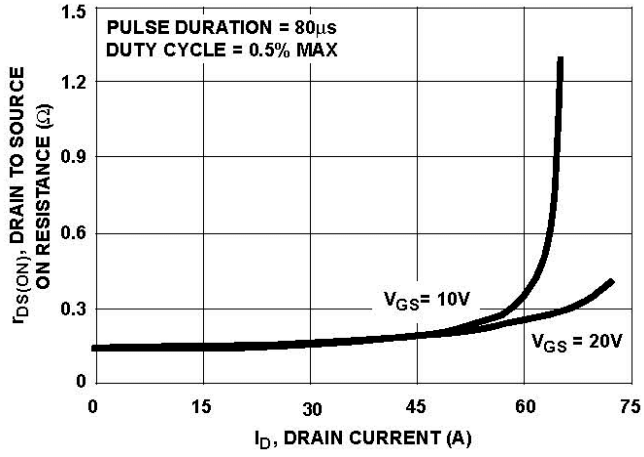


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

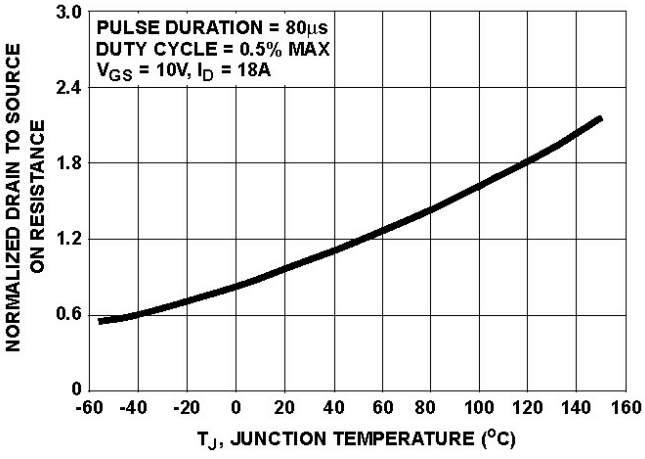


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

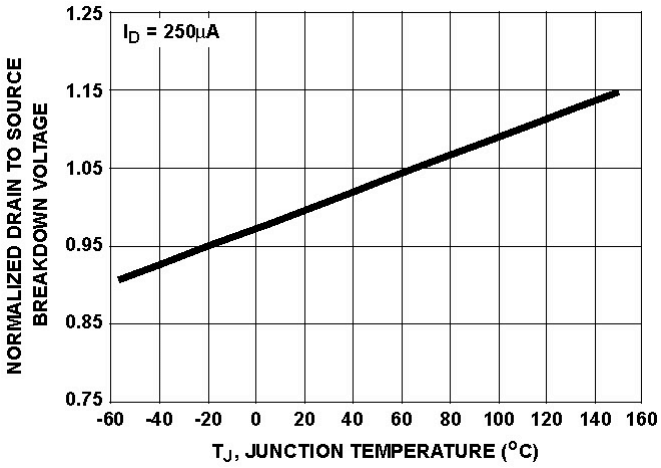


FIGURE10. NORMALIZED DRAIN TO SOURCE BREAKDOWN

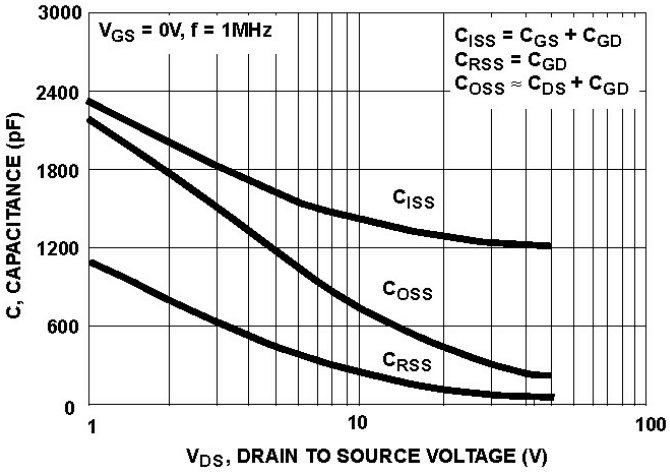


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

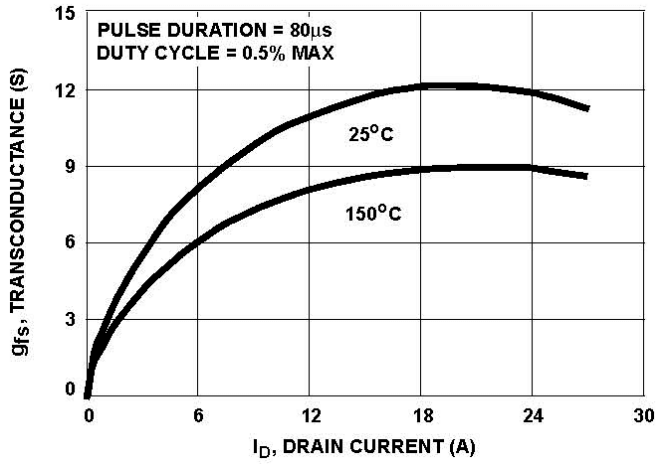


FIGURE 12. TRANSCONDUCTANCE VS DRAIN CURRENT

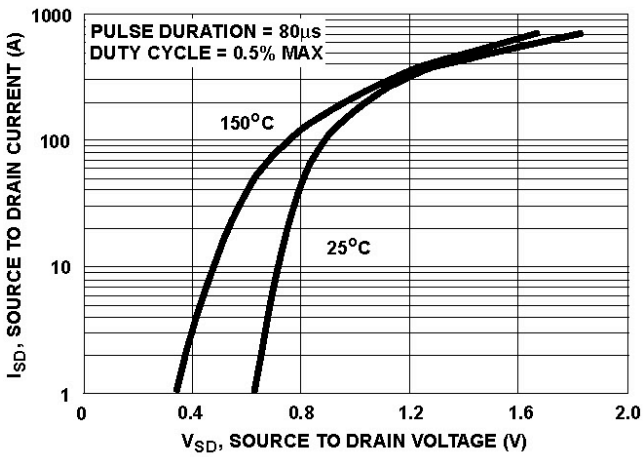


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

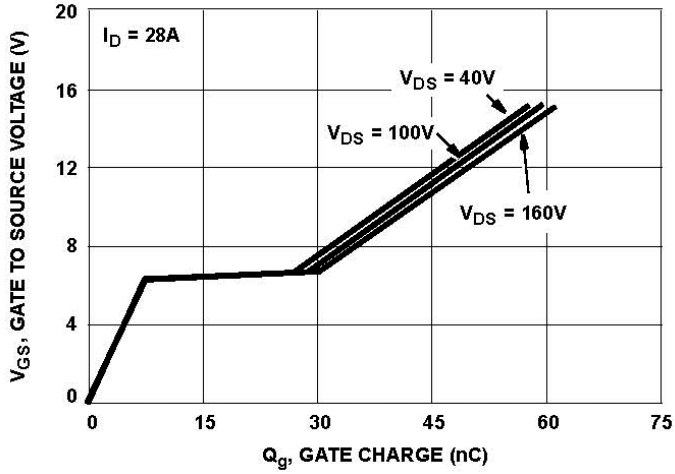


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

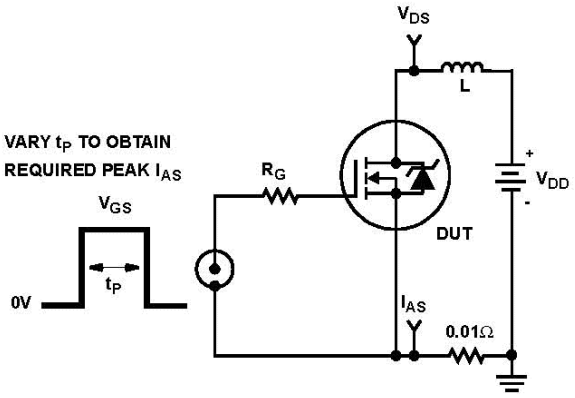


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

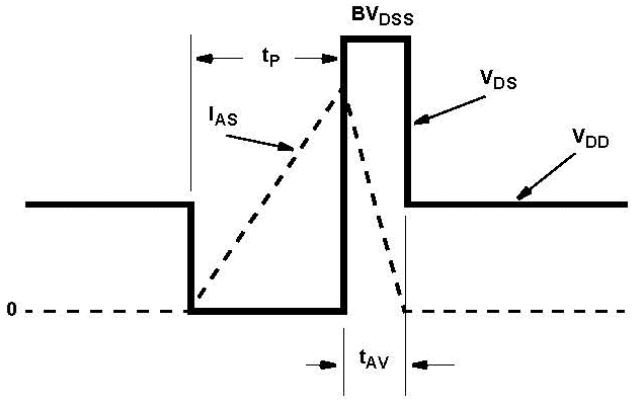


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

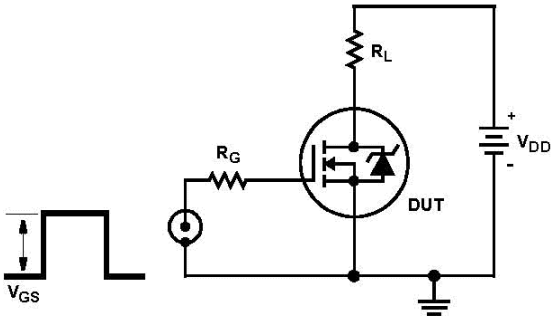


FIGURE 17. SWITCHING TIME TEST CIRCUIT

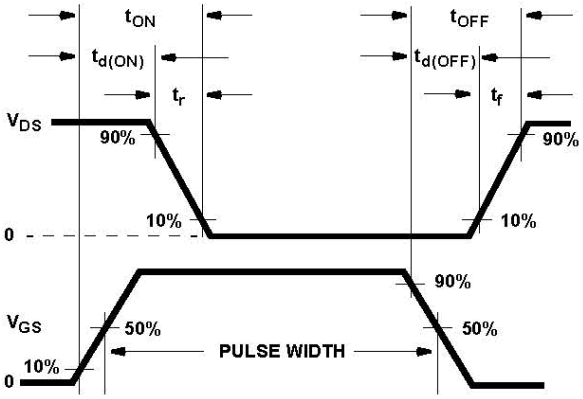


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

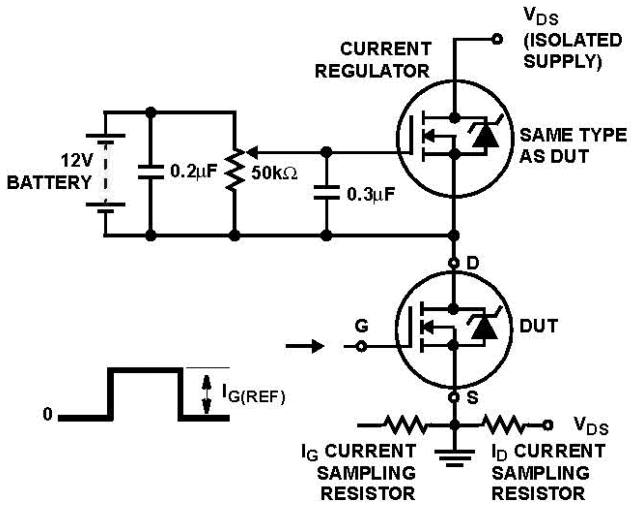


FIGURE 19. GATE CHARGE TEST CIRCUIT

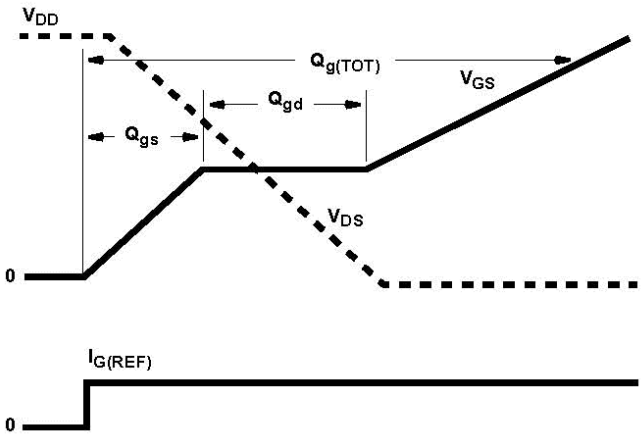


FIGURE 20.GATE CHARGE WAVEFORMS